* NOTICES *

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the structure of the sample for detecting electrically the influence of the stack structure in the multilayer-interconnection structure of a semiconductor device, and (a) is the cross section of this sample and (b) is some perspective diagrams of the sample of (a).
[Drawing 2] It is the property view showing the solution technical problem of this invention, and the graph showing the relation of the elevated-temperature reserve time of a sample and percent defective which show (a) to drawing 1 , and (b) are the graphs showing the relation between the wiring width of face after elevated-temperature preservation of the sample shown in drawing 1 , and resistance change.
[Drawing 3] It is the property view showing the solution technical problem of this invention, and is the graph which shows the relation of the storage temperature of a sample and accumulation failure attainment time which are shown in drawing 1 .
[Drawing 4] It is the property view showing the solution technical problem of this invention, and is drawing showing the relation between wiring structure and the rate of an excellent article.
[Drawing 5] It is the wiring structure shown in drawing 1 , and is the cross section showing the result which observed what became poor after elevated-temperature preservation with the transmission electron microscope.
[Drawing 6] (a) and (b) are drawings showing the result which carried out the simulation of the internal stress produced at the time of a temperature change with the finite element method in the wiring structure of drawing 5 .
[Drawing 7] It is drawing for explaining the 1st operation gestalt of this invention, and is the graph which shows the relation between the lap degree of an upper layer side plug and a lower layer side plug, and the rate of an excellent article.
[Drawing 8] The cross section showing the multilayer-interconnection structure of the semiconductor device which (a) requires for the 2nd operation gestalt of this invention, and (b) are graphs which show the relation between a recess d1 and a percent defective.
[Drawing 9] (a) - (f) is the process cross section showing the manufacture method of the multilayer-interconnection structure of the semiconductor device concerning the 3rd operation gestalt of this invention.
[Drawing 10] It is drawing for explaining the experiment concerning the 3rd operation gestalt of this invention, and drawing showing the cross-section structure of a sample where (a) was used for the experiment, and (b) are graphs which show the relation between the deposition temperature at the time of sputtering, and the depth d2 of the wiring crevice on a lower layer side plug.
[Drawing 11] (a) - (e) is the process cross section showing the manufacture method of the multilayer-interconnection structure of the semiconductor device concerning the 4th operation gestalt of this invention.
[Drawing 12] It is the cross section showing the multilayer-interconnection structure of the semiconductor device concerning the 5th operation gestalt of this invention.
[Drawing 13] It is drawing for explaining the 6th operation gestalt of this invention, and is the graph which shows the relation between the thickness of a wiring lower layer Ti film, and a percent defective.
[Description of Notations]
1 Semiconductor Substrate
2 1st Insulator Layer
2a Contact opening (the 1st opening)
3 Contact Pad Metal (Lower Layer Side Plug)
4 1st Wiring (Wiring Formed in Wiring Layer of 1)
4a Ti film (high-melting point metal membrane)
4c TiN film (film of a refractory metal or a refractory-metal alloy)
4H Lobe
4I Concavity
5 2nd Insulator Layer
5a Through hole opening (the 2nd opening)
6 Through Hole Pad Metal (Upper Layer Side Plug)
7 2nd Wiring (the Upper Wiring)
40 Void

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the multilayer-interconnection structure and its manufacture method of a semiconductor device.
[0002]
[Description of the Prior Art] In recent years, it originates in detailed-ization of the wiring in a VLSI, and the problem of the fall of the reliability of wiring has arisen. Although the structure established by carrying out phase opposite on both sides of wiring and the so-called stack structure are especially used for the upper surface and the inferior surface of tongue of wiring of the plug which consists of refractory metals, such as W (tungsten) and TiN, or a compound of those by progress of multilayering of wiring in multilayer-interconnection structure, in this stack structure, there is a problem of [wiring / of the portion pinched by the plug] a low in reliability.
[0003] In order to prevent the stress migration that wiring is disconnected with the stress from a protective coat, for example as 1st conventional example as a method of raising the reliability of wiring While forming the big wiring layer of grain size in the field to which the great portion of current flows, forming the small wiring layer of grain size in the position which tends comparatively] to require stress, such as the circumference (especially the side-attachment-wall section and the upper-limit section) of wiring, is performed (refer to JP,5-275426,A).
[0004] moreover -- as the 2nd conventional example -- a stack structure -- setting -- the width of face of wiring -- lower layer side connection -- the width of face of a hole -- narrow -- carrying out -- and upper layer side connection -- the pars basilaris ossis occipitalis of a hole -- lower layer side connection -- even a hole is made to extend and reinforcing it, as wiring is surrounded is proposed (refer to JP,8-167609,A)
[0005]
[Problem(s) to be Solved by the Invention] However, in the 1st conventional example, in order to form the small wiring layer of grain size in the side attachment wall of the big wiring layer of grain size and to form wiring, the width of face of wiring becomes large too much, and it is not fit for detailed-ization.
[0006] moreover -- the 2nd conventional example -- first -- an upper layer side and lower layer side connection -- since it is indispensable that the width of face of a hole is larger than the width of face of wiring, this is not fit for detailed-ization, either Furthermore, although wiring will be surrounded with a refractory metal or its compound, about stress with the refractory metal around wiring, or its compound, consideration is not made at all.
[0007] In view of the aforementioned problem, this invention makes it a technical problem to suppress the fall of the reliability of wiring, and the fall of the reliability of wiring resulting from the stress in the field especially inserted into the upper layer side plug and the lower layer side plug in the multilayer-interconnection structure of a semiconductor device of having a stack structure.
[0008]
[Means for Solving the Problem] In order to solve the aforementioned technical problem, the solution means which invention of a claim 1 provided The wiring layer more than two-layer [which was formed on a substrate and this substrate as multilayer-interconnection structure of a semiconductor device], The upper layer side plug which connects electrically the wiring formed in the wiring layer of one of the wiring layers more than two-layer [aforementioned], and its upper wiring, On both sides of the aforementioned upper layer side plug and the aforementioned wiring, phase opposite is carried out, and it is prepared, and has the lower layer side plug which connects electrically the aforementioned wiring, its lower layer wiring, or the aforementioned substrate. the aforementioned wiring It constitutes so that it may not have the grain boundary to the field inserted into the aforementioned upper layer side which carries out phase opposite, and the lower layer side plug.
[0009] The solution means which invention of a claim 2 provided moreover, as multilayer-interconnection structure of a semiconductor device The upper layer side plug which connects electrically the wiring formed in the wiring layer of one among the substrate, the wiring layer more than two-layer [which was formed on this substrate], and the wiring layer more than two-layer [aforementioned], and its upper wiring, On both sides of the aforementioned upper layer side plug and the aforementioned wiring, carry out phase opposite, and it is prepared, and has the lower layer plug which connects electrically the aforementioned wiring, its lower layer wiring, or the aforementioned substrate. The concavity which the aforementioned upper layer side plug contacts is formed in the upper surface of the wiring layer of the above 1, and the depth which caves in

from the upper surface of the wiring layer of the above 1 of this concavity is set to or less about 1 of the path of the aforementioned upper layer side and a lower layer side plug / 3.
[0010] Moreover, the wiring layer more than two-layer [by which the solution means which invention of a claim 3 provided was formed on a substrate and this substrate], The upper layer side plug which connects electrically the wiring formed in the wiring layer of one of the wiring layers more than two-layer [aforementioned], and its upper wiring, On both sides of the aforementioned upper layer side plug and the aforementioned wiring, phase opposite is carried out, and it is prepared, and has the lower layer side plug which connects electrically the aforementioned wiring, its lower layer wiring, or the aforementioned substrate. The aforementioned wiring, The difference of one [at least] coefficient of thermal expansion of material the aforementioned upper layer side and of the lower layer side plugs is made small to the grade which a void does not produce to the field inserted into the aforementioned upper layer side of the aforementioned wiring, and the lower layer side plug.
[0011] And in invention of a claim 4, either [at least] the wiring side in the multilayer-interconnection structure of the semiconductor device of the aforementioned claim 3, an upper layer side or of the lower layer side plugs shall be formed of the same material.
[0012] Furthermore, in invention of a claim 5, either [at least / both] the wiring side in the multilayer-interconnection structure of the semiconductor device of the aforementioned claim 4, an upper layer side or of the lower layer side plugs shall consist of aluminum or an aluminium alloy, or they shall consist of a laminated structure with aluminum or an aluminium alloy, refractory metals and refractory-metal alloys, or these compound layers.
[0013] The solution means which invention of a claim 6 provided moreover, as multilayer-interconnection structure of a semiconductor device The upper layer side plug which connects electrically the wiring formed in the wiring layer of one of a substrate, the wiring layer more than two-layer [which was formed on this substrate], and the wiring layers more than two-layer [aforementioned], and its upper wiring, On both sides of the aforementioned upper layer side plug and the aforementioned wiring, phase opposite is carried out, and it is prepared, and has the lower layer side plug which connects electrically the aforementioned wiring, its lower layer wiring, or the aforementioned substrate. the wiring layer of the above 1 The high-melting point metal membrane is formed in the inferior-surface-of-tongue side, and the thickness of this high-melting point metal membrane is set as 10nm or less or 80nm or more.
[0014] The solution means which invention of a claim 7 provided moreover, as the manufacture method of the multilayer-interconnection structure of a semiconductor device The process which forms the 1st opening in the 1st insulator layer formed on the substrate, and forms a lower layer side plug in this 1st opening, The 2nd insulator layer is formed the process which forms wiring on the 1st insulator layer of the above, and a lower layer side plug, and on the aforementioned wiring. It has the process which forms in this 2nd insulator layer the 2nd opening which counters the 1st opening of the above, and forms an upper layer side plug in it at this 2nd opening. the aforementioned lower layer side plug formation process Using the CMP method or the etchback method, it carries out so that the distance of the upper surface of the aforementioned lower layer side plug and the upper surface of the 1st insulator layer of the above may become or less about 1 of the path of the aforementioned upper layer side and a lower layer side plug / 3.
[0015] The solution means which invention of a claim 8 provided moreover, as the manufacture method of the multilayer-interconnection structure of a semiconductor device The process which forms the 1st opening in the 1st insulator layer formed on the substrate, and forms a lower layer side plug in this 1st opening, The process which forms the wiring which has the layer which consists of aluminum or an aluminium alloy at least on the 1st insulator layer of the above, and a lower layer side plug, Form the 2nd insulator layer on the aforementioned wiring, and the 2nd opening which counters the 1st opening of the above at this 2nd insulator layer is formed. This 2nd opening is equipped with the process which forms an upper layer side plug. the aforementioned wiring formation process The aforementioned wiring forms the aluminum of the aforementioned wiring, or the layer of an aluminium alloy in the field inserted into the aforementioned upper layer side which carries out phase opposite, and the lower layer side plug in the deposition temperature of about 200 degrees C or more by sputtering so that it may not have the grain boundary.
[0016]
[Embodiments of the Invention] Drawing 1 is drawing showing the structure of the sample for detecting electrically the influence of the stack structure in the multilayer-interconnection structure of a semiconductor device.
[0017] Drawing 1 (a) is the cross section of this sample. The contact pad metal with which 1 consists of W (tungsten) by which a semiconductor substrate and 2 were formed in the 1st insulator layer, and 3 was formed on the two-layer film of Ti and TiN in drawing 1 (a) (lower layer side plug), The 1st wiring which consists of an aluminum alloy containing Cu which 4 is formed on the two-layer film of Ti and TiN, and has a TiN film in the upper layer, The through hole pad metal which consists of the metal composition as the contact pad metal 3 with the 2nd insulator layer and 6 (upper layer side plug), [same / 5] As for the 2nd wiring as upper wiring which consists of the metal membrane composition as the 1st wiring 4 with 7 same], and 8, the silicon nitride as a protective coat and 9 are the polyimide films of an LSI chip coat.
[0018] Drawing 1 (b) is the perspective diagram of the portion containing the contact pad metal 3 and the through hole pad metal 6 which were connected to the 1st wiring 4 and its upper and lower sides among the samples of drawing 1 (a). By this sample, the wire length of the 1st wiring 4 is 31mm, and a contact hole and 1000 through holes are prepared at a time, respectively. The wiring width of face of the wiring 4 of the 1st of each sample is 0.4 micrometers - 1.0 micrometers in various sizes, and the diameter of a contact hole and a through hole is equal to wiring width of face.
[0019] A voltage-current property is measured among the pad sections 4A and 4B prepared in the ends of the 1st wiring 4.

Measurement of this voltage-current property is equivalent to measuring the resistance of the 1st wiring 4 which has the contact hole pad metal 3 and the through hole pad metal 6 up and down. Since the semiconductor substrate 1 electrically connected with the contact pad metal 3 consists of Si, the 2nd wiring 7 to which resistance was highly connected with the through hole pad metal 6 electrically as compared with the 1st wiring 4 which consists of a metal is because it is the structure which each became independent of electrically in the wiring layer.

[0020] Drawing 2 is drawing showing the result which measured pad section 4A and the voltage-current property between 4B, i.e., change of resistance of the 1st wiring 4, before and after elevated-temperature preservation of nearly 250 degrees C to the sample shown in drawing 1 . Among this drawing, (a) is a graph showing the relation between the time which saved the sample at 250 degrees C, and the percent defective of wiring, vertical axes are (%) and a percent defective and a horizontal axis is a 250-degree C reserve time (h). Here, it judges that the wiring whose resistance change exceeded 20% is poor, and is asking for the percent defective. Moreover, (b) is a graph showing the relation of wiring width of face and its resistance change after saving a sample at 250 degrees C for 1000 hours, a vertical axis is resistance (%) and change and a horizontal axis is wiring width of face (micrometer).

[0021] Drawing 3 is a graph which shows the relation of time, i.e., accumulation failure attainment time, until storage temperature and an accumulation failure rate become 0.1% to the sample shown in drawing 1 . Here, resistance change has judged that wiring exceeding 20% is poor like drawing 2 . A vertical axis is accumulation failure attainment time (h), and a horizontal axis is 1000-/storage temperature (1/K). When storage temperature of drawing 3 is near 250 degree C, accumulation failure attainment time shows the bird clapper smallest. Drawing 3 shows that resistance change of this wiring is a thing resulting from the defect by the migration of aluminum alloy by stress, and a stress migration poor [so-called].

[0022] Drawing 4 is drawing showing the relation between wiring structure and the rate of an excellent article. Drawing 4 shows the rate of an excellent article after saving for 1000 hours in 200 degrees C to three kinds of wiring structures of the wiring structure A where the upper layer side plug which carries out phase opposite as shown in drawing 1 , and the lower layer side plug were formed, the wiring structure B where only the lower layer side plug was formed, and the wiring structure C where only the upper layer side plug was formed. Here, it judges that the wiring whose resistance change exceeded 20% is poor, and is asking for the rate of an excellent article. Drawing 4 shows that the solution technical problem of this invention is a problem characteristic of the wiring structure where the upper layer side plug which carries out phase opposite, and the lower layer side plug were formed.

[0023] Drawing 5 is the wiring structure where the upper layer side plug which carries out phase opposite as shown in drawing 1 , and the lower layer side plug were formed, and is the cross section showing the result which observed that to which resistance change exceeded 20% after saving in 200 degrees C for 1000 hours with the transmission electron microscope. Drawing 5 also shows collectively the result which measured the crystallinity of aluminum alloy of the 1st wiring 4 according to the X diffraction.

[0024] As shown in drawing 5 , the void 40 was observed in the 1st wiring 4 inserted with the contact hole pad metal 3 as a lower layer side plug, and the through hole pad metal 6 as an upper layer side plug. moreover, the field direction of aluminum alloy in the wiring portions 43 and 44 pinched to the field direction of aluminum alloy in the wiring portions 41 and 42 pinched by the 1st insulator layer 2 and 2nd insulator layer 5 being (111) with the contact hole pad metal 3 and the through hole pad metal 6 -- or (311) (022) -- it was . Furthermore, there is the grain boundary 45 in the field across which it faced with the contact hole pad metal 3 and the through hole pad metal 6, and, thereby, the size of the crystal grain of the wiring portions 43 and 44 is smaller than the crystal grain in the wiring portions 41 and 42.

[0025] Drawing 6 is drawing showing the result which carried out the simulation of the internal stress produced when changing temperature to 25 degrees C from 400 degrees C with the finite element method about the field X of a right half among the portions pinched with the contact hole pad metal 3 and the through hole pad metal 6 in the wiring structure of drawing 5 .

[0026] The stress concerning the flat portion of the 1st wiring 4 is 200-300MPa (megger Pascal). On the other hand, the stress produced into the portion to which the through hole pad metal 6 advanced into the 1st wiring 4 was far high, when the upper surface of the contact pad metal 3 was below the upper surface of the 1st insulator layer 2 (drawing 6 (a)), it was 457MPa(s), and they were 449MPa(s) when the upper surface of the contact pad metal 3 was as flat-tapped as the upper surface of the 1st insulator layer 2 (drawing 6 (b)).

[0027] It is thought that the poor stress migration in the multilayer-interconnection structure of the semiconductor device concerning this invention is produced from these experiments and a simulation according to the following factors. Namely, it sets into the pinched wiring portion. (2) -- stress strong in the case of the structure to which the upper layer side plug advanced into wiring especially -- starting -- (3) -- the crystal grain of this wiring portion is small -- and a crystal-face direction (311) -- ** (022) -- it originates in it being a weak field direction to the said stress, and it is assumed that a stress migration will arise if elevated-temperature preservation is performed

[0028] Hereafter, the operation gestalt of this invention is explained with reference to a drawing.

[0029] (1st operation gestalt) The 1st operation gestalt of this invention makes small the lap degree of the upper layer side plug when seeing from [of a substrate side] a perpendicular, and a lower layer side plug to the wiring structure of having the upper layer side plug which carries out phase opposite, and a lower layer side plug, and makes stress concerning wiring small.

[0030] Drawing 7 is drawing showing the relation between the lap degree of an upper layer side plug and a lower layer side

plug, and the rate of an excellent article in the wiring structure of having the upper layer side plug which carries out phase opposite, and a lower layer side plug. the path of an upper layer side and a lower layer side plug sets to 0.6 micrometers, a lap degree is changed with 0.6 micrometers, 0.3 micrometers, and 0.2 micrometers here, and it is (that is, the distance between the center of the contact surface of the upper layer side plug and wiring when seeing from [of a substrate side] a perpendicular and the center of the contact surface of a lower layer side plug and wiring is changed with 0 micrometer, 0.3 micrometers, and 0.4 micrometers -- making) Moreover, when this wiring is saved in 200 degrees C for 1000 hours, the rate of an excellent article judges that that to which resistance change exceeded 20% is poor, and it is asking for it.

[0031] As shown in drawing 7 , when a lap degree was 0.2 micrometers, and the rate of an excellent article became 100% and set the lap degree to 0.2 micrometers or less, it turns out that a poor stress migration does not arise. Therefore, the good multilayer-interconnection structure which a poor stress migration cannot produce easily can be formed by making distance between the centers of the contact surface of an upper layer side plug and wiring, and the contact surface of a lower layer side plug and wiring into or more about 2 of the path of the 0.4-micrometer or more, i.e., the upper layer, side and a lower layer side plug / 3.

[0032] (2nd operation gestalt) Drawing 8 (a) is the cross section showing the multilayer-interconnection structure of the semiconductor device concerning the 2nd operation gestalt of this invention.

[0033] The multilayer-interconnection structure of the semiconductor device shown in drawing 8 (a) is manufactured as follows. First, after preparing contact opening as the 1st opening in the 1st insulator layer 2 on a semiconductor substrate by dry etching and forming the two-layer film of Ti and TiN by the spatter etc., W is embedded by the CVD method. And etchback of the two-layer film of W, and Ti and TiN is carried out, and the contact pad metal 3 (lower layer side plug) is formed in contact opening. Moreover the two-layer film of Ti and TiN is formed, aluminum alloy containing Cu is formed on this two-layer film, further, on it, a TiN film is formed and the 1st wiring 4 is formed. The 2nd insulator layer 5 is formed after the 1st wiring 4, and the through hole pad metal 6 (upper layer side plug) is formed in through hole opening as the 2nd opening like formation of the contact pad metal 3.

[0034] In the multilayer-interconnection structure of the semiconductor device shown in drawing 8 (a), the amount of over-etching at the time of carrying out etchback of the two-layer film of W, and Ti and TiN at the time of lower layer side plug formation was changed, and two or more samples from which a recess d1 differs were manufactured. A recess d1 is height which projects to the lower layer side formed in the inferior surface of tongue of a wiring layer in which the 1st wiring 4 was formed, and projects from the inferior surface of tongue of this wiring layer that is lobe 4H which the contact pad metal 3 contacts. Drawing 8 (b) is a graph which shows the percent defective when saving these samples in 250 degrees C for 168 hours. Here, it judges that that to which resistance change exceeded 20% is poor, and is asking for the percent defective. In drawing 8 (b), vertical axes are (%) and a percent defective and a horizontal axis is a recess (micrometer). Moreover, the path of an upper layer side and a lower layer side plug is 0.6 micrometers.

[0035] When a recess d1 is 0.2 micrometers or less so that clearly from drawing 8 (b), a percent defective becomes 0%, and a poor stress migration does not arise. The following was found when the cross section of the sample after percent-defective measurement was observed with the scanning electron microscope. In the sample with a larger recess d1 than 0.2 micrometers, the grain boundary almost surely existed in the field on the contact pad metal 3 in the 1st wiring 4. On the other hand, in the sample 0.2 micrometers or less, in the field on the contact pad metal 3 in the 1st wiring 4, a recess d1 hardly existed and the grain boundary's that of the size of the crystal grain of this field was almost the same as that of other fields.

[0036] From such a result, the time of a recess d1 being 0.2 micrometers is considered to be the boundary line of whether a poor stress migration arises. Therefore, the good multilayer-interconnection structure which a poor stress migration cannot produce easily can be formed by making a recess d1 into or less about 1 of the path of the 0.2-micrometer or less, i.e., the upper layer, side and a lower layer side plug / 3.

[0037] In addition, although the case where the etchback method by dry etching was used was shown when forming the contact pad metal 3 and the through hole pad metal 6, in using the etchback method, in order that a residue may tend to remain, over-etching increases, and there is an inclination for a recess d1 to become large. On the other hand, when forming the contact pad metal 3 and the through hole pad metal 6 using the CMP (Chemical Mechanical Polishing) method, the size of a recess d1 can be controlled with a sufficient precision. Therefore, the multilayer-interconnection structure of the semiconductor device concerning this operation gestalt can be formed certainly.

[0038] (3rd operation gestalt) Drawing 9 is drawing showing the manufacture method of the multilayer-interconnection structure of the semiconductor device concerning the 3rd operation gestalt of this invention, and is the cross section of the structure in each process. As shown in drawing 9 (a), contact opening 2a as the 1st opening is formed in the 1st insulator layer 2 on the semiconductor substrate 1, and as shown in drawing 9 (b), W film 3b is formed on two-layer film 3a of Ti and TiN on it. As shown in drawing 9 (c), two-layer film 3a of Ti and TiN on the 1st insulator layer 2 and W film 3b are **********ed, it leaves two-layer film 3a of Ti and TiN, and W film 3b only to contact opening 2a, and the contact pad metal 3 is formed by this. Moreover two-layer film 4a of Ti and TiN is formed, aluminum alloy 4b containing Cu is formed on this two-layer film 4a, TiN film 4c is further formed on it, and the 1st wiring 4 is formed.

[0039] aluminum alloy 4b is formed by sputtering, and deposition temperature at this time is made into 200 degrees C or more. It is hard coming to generate the grain boundary on contact opening 2a by depositing aluminum alloy 4b at the temperature of 200 degrees C or more. Moreover, aluminum alloy 4b is formed so that the depression on contact opening 2a may be filled, and the thickness of the portion on contact opening 2a becomes thicker than other portions.

[0040] As shown in drawing 9 (d), the 2nd insulator layer 5 is formed on the 1st wiring 4, through hole opening 5a as the 2nd opening is prepared in the 2nd insulator layer 5, and W film 6b is formed on two-layer film 6a of Ti and TiN. It is made for through hole opening 5a not to enter deeply in the 1st wiring 4 more than the level difference of the upper surface of the 1st insulator layer 2, and the upper surface of the KONTANTO pad metal 3 at this time. By forming through hole opening 5a in this way, the 1st wiring 4 serves as thickness of the portion of others [thickness / on the contact pad metal 3] more than equivalent.
[0041] Next, as shown in drawing 9 (e), two-layer film 6a of Ti and TiN on the 2nd insulator layer 5 and W film 6b are **********ed, it leaves two-layer film 6a of Ti and TiN, and W film 6b only to through hole opening 5a, and the through hole pad metal 6 is formed by this. Moreover two-layer film 7a of Ti and TiN is formed, aluminum alloy 7b containing Cu is formed on this two-layer film 7a, TiN film 7c is further formed on it, and the 2nd wiring 7 is formed. As shown in drawing 9 (f), the silicon nitride 8 is formed as a protective coat by plasma CVD.
[0042] Thus, in the multilayer-interconnection structure of the manufactured semiconductor device, aluminum alloy 4b of the 1st wiring 4 becomes the thickness of the portion of others [thickness / on the contact pad metal 3] more than equivalent. And like the 2nd operation gestalt, to aluminum alloy 4b of the field inserted into the field [on the contact pad metal 3 of the 1st wiring 4], i.e., the upper layer which carries out phase opposite, side, and the lower layer side plug, the grain boundary hardly existed and that of the size of the crystal grain of this field was almost the same as that of other fields. For this reason, with the structure concerning this operation gestalt, elevation of the wiring resistance by the poor stress migration after elevated-temperature preservation was not seen like the 2nd operation gestalt.
[0043] Drawing 10 is drawing showing the relation between the deposition temperature at the time of sputtering, and the thickness of the 1st wiring 4 in the field inserted into the upper layer side which carries out phase opposite, and the lower layer side plug. Drawing 10 (a) is drawing showing the cross-section structure of the sample used for the experiment for asking for this relation. The contact pad metal 3 which consists of W which formed contact opening of the diameter of 0.6 micrometer in the 1st insulator layer 2 of 0.7-micrometer ** on the semiconductor substrate 1, and was formed on the two-layer film of Ti and TiN at this contact opening is formed. The distance of the inferior surface of tongue of the 1st wiring 4 and the upper surface of the contact pad metal 3 is 0.2 micrometers. And on this, Ti film of 50nm **, aluminum alloy of 600nm ** containing Cu, and the TiN film of 30nm ** are formed. In this experiment, the deposition temperature of aluminum alloy was changed, the sample was manufactured, SEM observation of the cross section was carried out, and the depth d2 of concavity 4I of the 1st wiring 4 on the contact pad metal 3 was measured.
[0044] Drawing 10 (b) is a graph which shows this experimental result. In order to form aluminum alloy of the 1st wiring 4 in the field on contact opening more thickly than [other fields and] equivalent, the depth d2 needs to be 0.2 micrometers or less. Thus, the big stress produced when an upper layer side plug as shown in the stress simulation of drawing 6 advances into a wiring layer can be decreased by setting the depth d2 of concavity 4I to 0.2 micrometers or less. Therefore, the good multilayer-interconnection structure which a poor stress migration cannot produce easily can be formed by making the depth d2 into or less about 1 of the path of the 0.2-micrometer or less, i.e., the upper layer, side and a lower layer side plug / 3. As drawing 10 (b) shows, it is a time of the deposition temperature of aluminum alloy being 200 degrees C or more that the depth d2 is set to 0.2micro or less. Therefore, in order to make it wiring not have the grain boundary to the field inserted into the upper layer side which carries out phase opposite, and the lower layer side plug, it can be said that the deposition temperature of aluminum alloy is desirable 200 degrees C or more.
[0045] (4th operation gestalt) Drawing 11 is drawing showing the manufacture method of the multilayer-interconnection structure of the semiconductor device concerning the 4th operation gestalt of this invention, and is the cross section of the structure in each process. As shown in drawing 11 (a), contact opening 2a as the 1st opening is formed in the 1st insulator layer 2 on the semiconductor substrate 1. And as shown in drawing 11 (b), 4d of Ti films is formed, on it, 500nm of aluminum alloys which made the dimethyl aluminum hydride material gas, and deposited 100nm of aluminum films and contained Cu by sputtering continuously at the deposition temperature of 260 degrees C with CVD is deposited at the deposition temperature of 400 degrees C, and layer 4e of CVD aluminum and aluminum alloy is formed. Furthermore on it, 4f of TiN films is formed. Layer 4e of 4d of Ti films, and CVD aluminum and aluminum alloy and 4f of TiN films are processed into a wiring configuration, and the 1st wiring 4 is formed. Since aluminum is embedded at contact opening 2a in order to form an aluminum film by CVD, the 1st wiring 4 on contact opening 2a becomes thick enough compared with other portions.
[0046] As shown in drawing 11 (c), the 2nd insulator layer 5 is formed on the 1st wiring 4, and through hole opening 5a as the 2nd opening is prepared in the 2nd insulator layer 5. As shown in drawing 11 (d), layer 7e of CVD aluminum and aluminum alloy is formed on 7d of Ti films, 7f of TiN films is formed on it, a wiring configuration is processed and the 2nd wiring 7 is formed. Subsequently, as shown in drawing 11 (e), the silicon nitride 8 is formed as a protective coat by plasma CVD.
[0047] Thus, in the multilayer-interconnection structure of the manufactured semiconductor device, the 1st wiring 4, and the contact pad metal 3 and the through hole pad metal 6 are both formed with the same aluminum alloy. That is, wiring, and the upper layer side which carries out phase opposite on both sides of this and a lower layer side plug are formed with the same material. for this reason, the stress concerning the field to which the upper layer side plug and the lower layer side plug were pinched by the upper layer side and the lower layer side plug compared with the structure formed with a different metal (for example, W) from wiring is boiled markedly, and becomes small For this reason, with the structure concerning this operation gestalt, elevation of the wiring resistance by the poor stress migration after elevated-temperature preservation was not seen.
[0048] In addition, with this operation gestalt, although CVD and sputtering performed the pad of aluminum alloy to contact

opening 2a or through hole opening 5a, only CVD may perform. Moreover, after forming aluminum alloy by sputtering, you may perform a pad by making aluminum alloy flow by heating or pressurization.

[0049] Moreover, if the difference of the coefficient of thermal expansion of material is small to the grade which a void does not produce by elevated-temperature preservation even if it is the case where the material of an upper layer side plug and a lower layer side plug differs from wiring, a poor stress migration will not be produced. Although the coefficients of thermal expansion of W are 4.3x10-6/K, and a poor stress migration arises with W plug to the coefficients of thermal expansion of aluminum being 23.8x10-6/K since the difference is large, it stops for example, generating a poor stress migration by using nickel (coefficient-of-thermal-expansion 13.1x10-6/K), Cu (coefficient-of-thermal-expansion 16.8x10-6/K), etc. as plug material.

[0050] Moreover, as for the difference of the coefficient of thermal expansion of material, either a wiring side, an upper layer side and of the lower layer side plugs may be small to the grade which a void does not produce by elevated-temperature preservation. For example, although the stress migration by the difference of a coefficient of thermal expansion will occur in aluminum wiring if the plug between wiring layers is formed by W when forming the multilayer-interconnection structure where lower layer wiring consists of an aluminum alloy, and the upper wiring consists of Cu, the poor stress migration of aluminum wiring can be prevented by changing this plug material to nickel or Cu.

[0051] (5th operation gestalt) Drawing 12 is the enlarged view of the field of the 1st wiring 4 inserted with the contact pad metal 3 and the through hole pad metal 6 in multilayer-interconnection structure of the semiconductor device concerning the 5th operation gestalt of this invention. With the multilayer-interconnection structure shown in drawing 12 , it comes to carry out the laminating of the TiN film 4c as a film of aluminum alloy 4b which added Ti film 4a and Cu and a refractory metal, or a refractory-metal alloy, and the 1st wiring 4 touches the through hole pad metal 6 as an upper layer side plug through TiN film 4c.

[0052] Fundamentally, the multilayer-interconnection structure shown in drawing 12 is manufactured like the method concerning the 3rd operation gestalt shown in drawing 9 . However, it leaves without removing TiN film 4c of the 1st wiring 4, in case through hole opening 5a is formed in the 2nd insulator layer 5 by dry etching etc.

[0053] According to the multilayer-interconnection structure of the semiconductor device concerning this operation gestalt, since the 1st wiring 4 and the through hole pad metal 6 touch through TiN film 4c, the stress by the through hole pad metal 6 is eased by this TiN film 4c. Therefore, generating of a void can be suppressed and the resistance elevation by the stress migration can be prevented.

[0054] (6th operation gestalt) In the sample of drawing 1 (a), Ti film as a high-melting point metal membrane was formed in the lower layer of the 1st wiring 4 instead of the two-layer film of Ti and TiN, a setting change of the thickness of this Ti film was made in 0-120nm, and the percent defective was measured, respectively. Drawing 13 is a graph which shows the relation of the thickness of Ti film and the percent defective which were obtained by such measurement. Here, each sample is saved in 250 degrees C for 168 hours, and it judges that that to which resistance change exceeded 20% is poor, and is asking for the percent defective.

[0055] When the thickness of Ti film is 50nm so that drawing 13 may show, a percent defective becomes the maximum and, as for a percent defective, Ti film is set to 0 in 0nm and 100nm or more. The reason the relation between the thickness of Ti film and a percent defective becomes like drawing 13 is considered as follows. The stress concerning the 1st wiring 4 is eased with Ti film, and the effect of this stress relaxation is so large that thickness is large. On the other hand, if there is a Ti film, Si in an aluminum containing alloy will be sucked out by Ti film 4a, and it will become easy to produce an opening (Vacancy) in an aluminum containing alloy. Therefore, it is considered by the balance of the effect of stress relaxation, and the ease of being generated of the opening in an aluminum containing alloy for the relation between the thickness of Ti film and a percent defective to become like drawing 13 .

[0056] Therefore, the good multilayer-interconnection structure which a poor stress migration cannot produce easily can be formed excepting the range of 10nm - 80nm as thickness of Ti film, i.e., by setting thickness of Ti film to 10nm or less or 80nm or more.

[0057] In addition, although explained taking the case of two-layer wiring structure, in the multilayer-interconnection structure of three or more layers, this invention is realizable with each operation gestalt, similarly.

[0058] Moreover, you may carry out each operation gestalt combining the either. For example, the distance between the centers of the contact surface of the center of the contact surface of an upper layer side plug and wiring, a lower layer side plug, and wiring is set combining the 1st operation gestalt and the 2nd operation gestalt to or more about 2 of the path of an upper layer side and a lower layer side plug / 3. And the height of the lobe which a lower layer side plug contacts formed in the inferior surface of tongue of a wiring layer may constitute the multilayer-interconnection structure set to or less about 1 of the path of an upper layer side and a lower layer side plug / 3. similarly combining the 2nd operation gestalt and the 3rd operation gestalt **** -- the 1- you may combine the 3rd operation gestalt

[0059]

[Effect of the Invention] As mentioned above, since the fall of the reliability of wiring resulting from the stress in the field inserted into the upper layer side plug and the lower layer side plug can be suppressed according to this invention, the resistance elevation by the stress migration can be suppressed.